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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,356	03/08/2001	Hidekazu Watanabe	80398P346	7422

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EXAMINER	
CERULLO, JEREMY S	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,356	WATANABE ET AL.	
	Examiner	Art Unit	
	Jeremy S. Cerullo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending in the following action.

Response to Arguments

2. Applicant's arguments filed 11 March, 2005, have been fully considered but they are not persuasive.

3. With regards to Applicant's arguments concerning the rejection of Claims 1-2, 11-12, and 21-22 as being unpatentable over Hubbins, the Examiner is not persuaded and maintains the rejections. Applicant argues that "Since the ports are inside the device, they cannot be master buses." The Examiner respectfully disagrees. One of ordinary skill in the art would know a bus to be "a set of hardware lines – wires – used for data transfer among the components of a computer system..." (Microsoft Press Computer Dictionary, Second Edition). Neither by this definition, nor by any other definition given in the disclosure, is a bus required to be external to a device. Furthermore, the communication lines between Ports A-B and Processors A-B, respectively, in Figure 1 of Hubbins, can be interpreted as master buses via which are coupled to the Multiplexer and the Arbitration logic via the Ports. Also the Applicant argues that there is no slave bus. Given the broadest reasonable interpretation of the art, the Examiner contends that the connection between the MUX and the memory (interpreted as a slave to the processors) is indeed a slave bus (a data bus for communicating with a slave device).

The Applicant also argues that using several devices in parallel does not mean that a plurality of slave buses exists. The Examiner respectfully disagrees. Given the broadest reasonable interpretation of the art, the Examiner interprets the communication lines for each slave device to be a separate slave bus (a data bus for communicating with a slave device).

4. With regards to Applicant's arguments concerning the rejection of Claims 3, 13, and 23 as being unpatentable over Hubbins in view of Burgess, the Examiner is not persuaded and maintains the rejections. Applicant restates arguments regarding Claims 1-2, 11-12, and 21-22 that have already been addressed (see discussion above). Applicant further argues that Burgess "merely discloses an address decoder to pair each slave device with a corresponding address selected line..." The Examiner agrees that this is what Burgess teaches, but the Examiner notes that is what the Applicant is claiming: "...the address decoder generating a device select signal."

5. With regards to Applicant's arguments concerning the rejection of Claims 4-5, 7-10, 14-15, 17-20, 24-25, and 27-30 as being unpatentable over Hubbins and Burgess in view of Opoczynski, the Examiner is not persuaded and maintains the rejections. Applicant restates arguments regarding Hubbins and Burgess that have already been addressed (see discussion above). Applicant further argues that Opoczynski "merely discloses a selector to control which of line drivers/receivers receives the serial port I/O stream." The Examiner agrees with this argument, but notes that selector of Opoczynski reads on the limitations of the claims, for one of ordinary skill in the art would know a multiplexer to be "a hardware circuit for selecting a single output from

multiple inputs..." (Microsoft Press Computer Dictionary, Second Edition), which is shown in both Figure 3 of Opoczynski and in Figure 3 of the instant application. The Applicant further argues that the Multiplexer of Figure 2 does not perform both the functions of a multiplexer and a de-multiplexer. The Examiner agrees with this argument, but while labeled a multiplexer, Item 21 of Figure 2 of Hubbins actually performs as a de-multiplexer, taking the output from the memory (slave device) and sending the data along one of two data buses, and therefore still reads over the Applicant's invention. The Examiner notes that the rejection is made over the entire piece of art, not limited to the Examiner's mapping of the limitations. The mapping of the limitations in the rejections below has been corrected, and the rejections are maintained.

6. With regards to Applicant's arguments concerning the rejection of Claims 6, 16, and 26 as being unpatentable over Hubbins, Burgess, and Opoczynski in view of Leedom, the Examiner is not persuaded and maintains the rejections. Applicant restates arguments regarding Hubbins, Burgess, and Opoczynski that have already been addressed (see discussion above). Applicant further argues that Leedom "merely discloses a common memory interface to a scalar/vector processor..." and that "a scalar/vector processor is not a slave device connected to a slave bus." The Examiner agrees that a scalar/vector processor is not a slave device connected to a slave bus, but the Examiner notes that he did not rely of that information for his rejection of the claims. The Examiner merely used Leedom's teaching of a common memory interface

in combination with the other art. Leedom teaches a common memory interface to allow multiple devices access to common memory, as is claimed by the Applicant.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and second processors to generate an arbitration select signal (Figure 1). Hubbins also

teaches a multiplexer coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to connect multiple arbiter/multiplexer units to the first and second processors. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

10. As for Claim 2, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

11. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

12. Claims 4-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S.

Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46). While labeled a multiplexer, Item 21 of Figure 2 of Hubbins actually performs as a de-multiplexer, taking the output from the memory (slave device) and sending the data along one of two data buses. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

13. As for Claim 5, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22).

14. As for Claim 7, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

15. As for Claim 8, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

16. As for Claim 9, Hubbins teaches that the first slave device is a memory device (Figure 1).

17. As for Claim 10, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

18. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

19. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and second processors to generate an arbitration select signal (Figure 1). Hubbins also teaches a multiplexer for providing device access information coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to connect multiple arbiter/multiplexer units to the first and second processors. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

20. As for Claim 12, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

21. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 11-12 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

22. Claims 14-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 13 above, and further in view of U.S. Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46). While labeled a multiplexer, Item 21 of Figure 2 of Hubbins actually performs as a de-multiplexer, taking the output from the memory (slave device) and sending the data along one of two data buses. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

23. As for Claim 15, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

24. As for Claim 17, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

25. As for Claim 18, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

26. As for Claim 19, Hubbins teaches that the first slave device is a memory device (Figure 1).

27. As for Claim 20, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

28. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 14-15 and 17-20 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

29. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,698,753 (Hubbins). Hubbins teaches an arbiter coupled to first and

second processors to generate an arbitration select signal (Figure 1). Hubbins also teaches a multiplexer for providing device access information coupled to the first and second processors and to a slave (in this case memory). While Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Abstract). It would be obvious to one of ordinary skill in the art at the time of the invention to combine multiple arbiter/multiplexer units (bus controllers) to the first and second processors in an interface circuit. One would be motivated to do so in order to allow for independent access to the slaves by each processor.

30. As for Claim 22, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

31. Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins as applied to claims 21-22 above, and further in view of U.S. Patent No. 5,590,369 (Burgess). Burgess teaches the additional limitation of an address decoder (Figure 1, Item 84) that decodes the slave address (Figure 1, Item 80) and generates a device select signal (Figure 1, Item 88). See Column 6, Lines 9-35 of Burgess. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an address decoder as taught by Burgess in the apparatus of Hubbins. The motivation for doing so would be to allow for multiple slaves on the slave bus, in addition to the RAM of Hubbins.

32. Claims 24-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 (Opoczynski). Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O (Figure 3, Item 46). While labeled a multiplexer, Item 21 of Figure 2 of Hubbins actually performs as a de-multiplexer, taking the output from the memory (slave device) and sending the data along one of two data buses. Therefore, Hubbins teaches the use of de-multiplexer to provide the bus response information to one of the first and second processors. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the selector of Opoczynski in the apparatus of Hubbins and Burgess. One would have been motivated to do so in order to further support multiple slaves on the slave bus, in addition to the RAM of Hubbins.

33. As for Claim 25, Hubbins also teaches that the device access information provided to the slave may be write data. (Column 3, Line 59 – Column 4, Line 22)

34. As for Claim 27, Hubbins teaches that a DMA can be used as a host (Column 11, Lines 29-37).

35. As for Claim 28, Hubbins teaches that a microprocessor can be one of the devices connected as a processor (Figure 12 and Column 11, Lines 13-28).

36. As for Claim 29, Hubbins teaches that the first slave device is a memory device (Figure 1).

37. As for Claim 30, Hubbins teaches a homogeneous set (all memory devices) (Figure 1).

38. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubbins, Bugress, and Opoczynski as applied to claims 24-25 and 27-30 above, and further in view of U.S. Patent No. 5,717,895 (Leedom). Leedom teaches access to common memory by various devices through a common memory interface (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the common memory and common memory interface of Leedom in the system taught by Hubbins, Bugress, and Opoczynski. One would have been motivated to do so in order to allow the various slave devices access to data that would need to be shared.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 7:00-4:30; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JSC

REHANA PERVEEN
PRIMARY EXAMINER
1/6/05